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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,974	12/09/2003	Takeyoshi Hisada	06-003	2200

23400 7590 06/09/2006

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,974	HISADA ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/729974 Attorney's Docket #: 06-003
Filing Date: 12/9/2003; claimed foreign priority to 12/19/2002

Applicant: Hisasa et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 8), filed 4/13/06, has been acknowledged.

This application contains claims 9 to 13 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3 and 5-8 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ueno (U.S. Patent # 6,948,944 B2).

I. Ueno (figures 1 to 19) specifically figure 18 show a metal wiring board comprising a metal plate **401** as a substrate, wherein: the metal plate is processed in a predetermined wiring pattern **102**; the metal plate has a surface including a soldering area and a non-soldering area; the soldering area is a conductive area prepared for electrical connection; and the non-soldering area is an electrically isolated area coated with solder resist **103**.

2. The metal wiring board according to claim 1, Ueno show wherein the predetermined wiring pattern includes a wiring portion that functions as an electrical wire.

3. The metal wiring board according to claim 1, Ueno show wherein the predetermined wiring pattern further includes a terminal portion for electrical connection with an external device.

5. The metal wiring board according to claim 1, Ueno show wherein the solder resist coating on the non-soldering area is performed by solder resist printing.

6. The metal wiring board according to claim 1, Ueno show wherein the wiring portions are held by a resin case **402** at ends thereof.

7. The metal wiring board according to claim 1, Ueno show wherein the soldering are is prepared for soldering of a surface mount device **104** having leads **403** with a small pitch.

8. The metal wiring board according to claim 1, Ueno show wherein: the metal plate includes a plurality of soldering areas; and the soldering areas are arranged so that a surface mount device bridges adjacent electrical wiring portions when soldered.

[0010] FIG. 18 is a cross-sectional view of a wiring board with a built-in electronic component, in which the wiring board has a heat dissipation function. The wiring board with a built-in electronic component includes a metal core substrate 401. Both a top surface and a bottom surface of the metal core substrate 401 are covered with an insulating resin layer 402. On the insulating resin layer 402 on both surfaces of the metal core substrate 401, an electronic component-mounting land as a part of a conductive pattern 102 and a solder resist layer 103 are provided. An electronic component 104 is provided on the solder resist layer 103 on the top surface of the metal core substrate 401. A terminal of the electronic component 104 is connected to the electronic component-mounting land via a solder member 106. The conductive pattern 102 on the top surface of the metal core substrate 401 and the conductive pattern 102 on the bottom surface of the metal core substrate 401 are electrically connected to each other via a through-hole 403.

Claims 1-3 and 5-8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Isawa et al. (Japan Patent # 2000-165045).

I. Isawa et al. (figures 1 to 10) specifically figures 1b and 4b show a metal wiring board comprising a metal plate as a substrate **1**, wherein: the metal plate is processed in a predetermined wiring pattern **5**; the metal plate has a surface including a soldering area **36xT** and a non-soldering area **(section under 7)**; the soldering area is a conductive

area prepared for electrical connection; and the non-soldering area is an electrically isolated area coated with solder resist **7**.

2. The metal wiring board according to claim 1, Isawa et al. show wherein the predetermined wiring pattern includes a wiring portion that functions as an electrical wire.

3. The metal wiring board according to claim 1, Isawa et al. show wherein the predetermined wiring pattern further includes a terminal portion for electrical connection with an external device.

5. The metal wiring board according to claim 1, Isawa et al. show wherein the solder resist coating on the non-soldering area is performed by solder resist printing.

6. The metal wiring board according to claim 1, Isawa et al. show wherein the wiring portions are held by a resin case **3** at ends thereof.

7. The metal wiring board according to claim 1, Isawa et al. show wherein the soldering are is prepared for soldering of a surface mount device having leads with a small pitch.

8. The metal wiring board according to claim 1, Isawa et al. show wherein: the metal plate includes a plurality of soldering areas; and the soldering areas are arranged so that a surface mount device bridges adjacent electrical wiring portions when soldered.

Initially, and with respect to claim 4, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ueno (U.S. Patent # 6,948,944 B2).

4. The metal wiring board according to claim 1, Ueno show wherein the processing of the metal plate id performed by stamping the metal plate.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Isawa et al. (Japan Patent # 2000-165045).

4. The metal wiring board according to claim 1, Ueno show wherein the processing of the metal plate id performed by stamping the metal plate.

As to the grounds of rejection under section 103, see MPEP § 2113.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/e23.178,668,699,732,774 439/68,67,71 361/836 174/262	6/6/06
Other Documentation: foreign patents and literature in 257/ e23.178,668,699,732,774 439/68,67,71 361/836 174/262	6/6/06
Electronic data base(s): U.S. Patents EAST	6/6/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/7/06